

## WHAT IS CLAIMED IS:

1           1.    For use in a shared bus system comprising a plurality of  
2 bus devices capable of requesting access to a shared bus, a bus  
3 arbitrator operable to slowly activate and rapidly de-activate  
4 tristate line drivers coupled to said shared bus, said bus  
5 arbitrator comprising:  
6                an input interface capable of receiving a first bus  
7 access request signal from a first of said plurality of bus  
8 devices;  
9                a delay circuit capable of receiving said first bus  
10 access request signal from said input interface and generating  
11 therefrom a time-delayed first bus access request signal; and  
12               a comparator circuit capable of receiving said first bus  
13 access request signal from said input interface and said time-  
14 delayed first bus access request signal from said delay circuit and  
15 generating a line driver enable signal only if both of said first  
16 bus access request signal and said time-delayed first bus access  
17 request signal are enabled.

1           2.    The bus arbitrator as set forth in Claim 1 wherein  
2 comparator circuit disables said line driver enable signal if  
3 either of said first bus access request signal and said time-  
4 delayed first bus access request signal is disabled.

1           3.    The bus arbitrator as set forth in Claim 2 wherein a time  
2 delay of said delay circuit is greater than a maximum de-activation  
3 delay period associated with said tri-state line drivers.

1           4.    The bus arbitrator as set forth in Claim 3 wherein said  
2 comparator circuit comprises an AND gate having a first input for  
3 receiving said first bus access request and a second input for  
4 receiving said time-delayed first bus access request signal.

1           5.    The bus arbitrator as set forth in Claim 3 wherein said  
2 delay circuit is an asynchronous delay circuit.

1           6.    The bus arbitrator as set forth in Claim 5 wherein said  
2 delay circuit comprises an even number of inverters connected in  
3 series, wherein a first of said even number of inverters receives  
4 said first bus access request signal from said input interface and  
5 a last of said even number of inverters generates said time-delayed  
6 first bus access request signal.

1           7.    The bus arbitrator as set forth in Claim 3 wherein said  
2 delay circuit is a synchronous delay circuit.

1           8.    The bus arbitrator as set forth in Claim 7 wherein said  
2 delay circuit comprises a flip-flop having an input capable of  
3 receiving said first bus access request signal from said input  
4 interface and an output coupled to said comparator circuit that  
5 generates said time-delayed first bus access request signal.

1           9.    A shared bus system comprising:

2                N bus devices capable of requesting access to a shared  
3 bus;

4                M tristate line drivers, each of said M tristate line  
5 drivers having an input for receiving a logic bit from one of said  
6 N bus devices and an output for outputting said received logic bit  
7 to said shared bus, wherein said each tristate line driver outputs  
8 said received logic bit when a line driver enable signal associated  
9 with said each tristate line driver is enabled and an output of  
10 said each tristate line driver is put into a high-impedance state  
11 when said line driver enable signal is disabled; and

12               a bus arbitrator operable to slowly activate and rapidly  
13 de-activate said M tristate line drivers, said bus arbitrator  
14 comprising:

15               an input interface capable of receiving a first bus  
16 access request signal from a first of said N bus devices;

17               a delay circuit capable of receiving said first bus  
18 access request signal from said input interface and generating  
19 therefrom a time-delayed first bus access request signal; and

20               a comparator circuit capable of receiving said first  
21 bus access request signal from said input interface and said  
22 time-delayed first bus access request signal from said delay

23 circuit and generating a line driver enable signal only if  
24 both of said first bus access request signal and said time-  
25 delayed first bus access request signal are enabled.

1 10. The shared bus system as set forth in Claim 9 wherein  
2 comparator circuit disables said line driver enable signal if  
3 either of said first bus access request signal and said time-  
4 delayed first bus access request signal is disabled.

1 11. The shared bus system as set forth in Claim 10 wherein a  
2 time delay of said delay circuit is greater than a maximum de-  
3 activation delay period associated with said tri-state line  
4 drivers.

1 12. The shared bus system as set forth in Claim 11 wherein  
2 said comparator circuit comprises an AND gate having a first input  
3 for receiving said first bus access request and a second input for  
4 receiving said time-delayed first bus access request signal.

1 13. The shared bus system as set forth in Claim 11 wherein  
2 said delay circuit is an asynchronous delay circuit.

1        14. The shared bus system as set forth in Claim 13 wherein  
2        said delay circuit comprises an even number of inverters connected  
3        in series, wherein a first of said even number of inverters  
4        receives said first bus access request signal from said input  
5        interface and a last of said even number of inverters generates  
6        said time-delayed first bus access request signal.

1        15. The shared bus system as set forth in Claim 11 wherein  
2        said delay circuit is a synchronous delay circuit.

3        16. The shared bus system as set forth in Claims 15 wherein  
4        said delay circuit comprises a flip-flop having an input capable of  
5        receiving said first bus access request signal from said input  
6        interface and an output coupled to said comparator circuit that  
7        generates said time-delayed first bus access request signal.

1        17. For use in a shared bus system comprising N bus devices  
2 capable of requesting access to a shared bus, a method for slowly  
3 activating and rapidly de-activating a plurality of tristate line  
4 drivers coupled between the shared bus and the N bus devices, the  
5 method comprising the steps of:

6            receiving a first bus access request signal from a first  
7 of the plurality of bus devices;

8            generating from the first bus access request signal a  
9 time-delayed first bus access request signal; and

10           comparing in a comparator circuit the first bus access  
11 request signal and the time-delayed first bus access request signal  
12 and generating a line driver enable signal only if both of the  
13 first bus access request signal and the time-delayed first bus  
14 access request signal are enabled.

1        18. The method as set forth in Claim 17 further comprising  
2 the step of disabling the line driver enable signal if either of  
3 the first bus access request signal and the time-delayed first bus  
4 access request signal is disabled.

1           19. The method as set forth in Claim 18 wherein a time delay  
2 associated with the time-delayed first bus access request signal is  
3 greater than a maximum de-activation delay period associated with  
4 the plurality of tri-state line drivers.

1           20. The shared bus system as set forth in Claim 19 wherein  
2 the comparator circuit comprises an AND gate having a first input  
3 for receiving the first bus access request and a second input for  
4 receiving the time-delayed first bus access request signal.